ABSTRACT

First and second IP cores are formed on one chip. Each of the first and second IP cores has metal layers. In the first IP core, an uppermost layer of the metal layers is thick and is a layer on which a core power source line is formed. In the second IP core, a metal layers equal in level to the uppermost layer in the first IP core becomes an intermediate layer. In the second IP core, thin intermediate layers are formed on this intermediate layer. Thin intermediate layers are layers on which signal lines are formed and have a narrow wiring pitch. In the second IP core, a layer on which a power source line is formed is provided on the thin intermediate layers.